Design of a Step-Down Switched-Capacitor AC/DC Converter Using Nested Voltage Equalizers

K. Eguchi, W. Do, and I. Oota

***Abstract*—A novel step-down switched-capacitor (SC) ac/dc converter using nested voltage equalizers is presented in this paper. Unlike the conventional SC ac/dc converters, the proposed converter consists of a full waveform rectifier with a big capacitor and nested voltage equalizers. In the nested voltage equalizers, a part of the capacitor voltage of the voltage equalizer is converted by other voltage equalizers to offer flexible conversion ratios, where each voltage equalizer is controlled by non-overlapped two-phase clock pulses. Therefore, the proposed converter can achieve not only simple circuit control but also flexible conversion ratios. Concerning the 1/9 step-down SC ac/dc converter, the advantages of the proposed converter was investigated by simulated program with integrated circuit emphasis (SPICE) simulations and experiments. The SPICE simulation demonstrated that the proposed converter can achieve higher power efficiency and lower ripple noise than conventional SC ac/dc converters. Furthermore, the feasibility of the proposed converter was confirmed by the experimental circuit implemented on a breadboard.**

***Keywords*—AC/DC converter, Step down converters, Switched capacitor converters, Voltage equalizers.**

I. Introduction

To develop small and light power converters, the switched-capacitor (SC) technique [1]-[9] is one of the most promising design methods. Among others, the ac/dc converter designed by SC techniques is the vital component of electrical devices. Although the SC ac/dc converter is not suitable for high power applications, it enables us to implement the power converter without a high turn ratio transformer. For this reason, the SC ac/dc converter has been studied over the past few decades. In 1989, Ueno et al. [1] proposed the first SC ac/dc converter. Owing to the bidirectional converter topology, this converter can realize step-up/step- down ac/dc conversion. However, due to the slow switching control, the 1st ac/dc converter suffers from large ripple noise. Based on this study, Oota et al. suggested the series-parallel type ac/dc converter [2]. However, due to the multi-phase clocking, the ripple noise of these converters is still large though the power efficiency is improved. To overcome this problem, we proposed a high-speed control method for the series-parallel type ac/dc converter [3]. By using the high-speed control technique, the power efficiency and ripple nose of the series-parallel type ac/dc converter are improved. However, this technique suffers from the complex switching control. To reduce inrush current, the ring-type ac/dc converter was developed by Terada et al. [4], [5]. Unlike the series-parallel type ac/dc converter, the ring-type ac/dc converter can provide not only small inrush current but also flexible conversion ratios. Following these studies, Hirakawa et al. proposed the digital-selecting type ac/dc converter [6]. Unlike the ring-type converter and the series-parallel type converter, the voltage ratio of capacitors is set to powers of 2 in the digital-selecting type ac/dc converter. For this reason, the digital-selecting type ac/dc converter can achieve more flexible conversion ratio than the ring-type converter. However, many circuit components are necessary to implement these ac/dc converters. To achieve small number of circuit components, Abe et al. proposed the series-connected ac/dc converter [7]. By connecting voltage equalizers [8], [9] in series, the series-connected converter offers the conversion ratios expressed by the multiplication form of conversion ratios of voltage equalizers. Therefore, the series-connected converter achieves a high step- down conversion ratio at small number of circuit components. However, there is still room for improvement in the point of power efficiency, ripple nose, conversion flexibility, etc.

In this paper, we propose a step-down SC ac/dc converter using nested voltage equalizers. The proposed converter consists of a full waveform rectifier with a big capacitor and nested voltage equalizers. By nesting the voltage equalizers proposed in [8], [9], the proposed converter converts a part of the capacitor voltage of a voltage equalizer by other voltage equalizers. By the nesting conversion, the conversion ratio of the proposed converter is expressed as a reverse value of the total sum of main capacitors' voltage ratios. In addition, the proposed topology can reduce the number of circuit components, because the voltage ratio of main capacitors is not equal by the nesting conversion. Therefore, the proposed converter can offer not only flexible conversion ratios but also small number of circuit components. Furthermore, non-overlapped two-phase clock pulses operate the voltage equalizer. Therefore, the proposed converter can achieve simple circuit control.

To confirm the validity of circuit design, simulated program with integrated circuit emphasis (SPICE) simulations and

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experiments are performed concerning the proposed converters realizing 1/9 step-down conversion. First, by using the SPICE simulator, the characteristic of the proposed converter is compared with that of conventional converters reported in [2] and [7]. Next, the experimental circuit of the proposed converter is assembled on a breadboard.

The rest of this paper is as follows: Section 2 describes the difference of circuit topology between the proposed converter and conventional converters [2], [7] to show the originality of the proposed SC ac/dc converter. Sections 3 and 4 describe the SPICE simulated results and experimental results to demonstrate the effectiveness of the proposed converter. Finally, the results of this study are summarized in section 5.

II. Circuit Configuration

A. Conventional Converter

The circuit configuration of the conventional SC ac/dc converter [7] is drawn in Fig.1. As Fig.1 shows, the conventional converter is composed of a full bridge circuit and two converter blocks. The circuit components of Fig.1 are 12 power switches, 9 capacitors, and 4 diodes. By converting V_{i1} twice, the conventional converter offers the following voltage:

$$V_{out} = \left(\frac{1}{3}\times\frac{1}{3}\right)V_i = V_{o1}\times\left(\frac{1}{3}\right)V_i = \left(\frac{1}{9}\right)V_{i1} \quad (1)$$

In (1), V_{i1} is the output voltage of the full bridge circuit, V_{o1} (= V_{i2}) is the output voltage of the converter block-1, and V_o (= V_{o2}) is the output voltage of the converter block-2. As (1) shows, the conversion ratio is expressed by the multiplication form of conversion ratios of the converter blocks. In each converter block, each input voltage is divided by the main capacitors $C_{i,2}$, $C_{i,3}$ and $C_{i,4}$ (i=1, 2). The electric charges stored in the main capacitors are equalized by connecting the flying capacitor $C_{i,1}$ in turn to the main capacitors. As shown in Fig.1, the switches of the conventional converter is controlled by three-phase clock

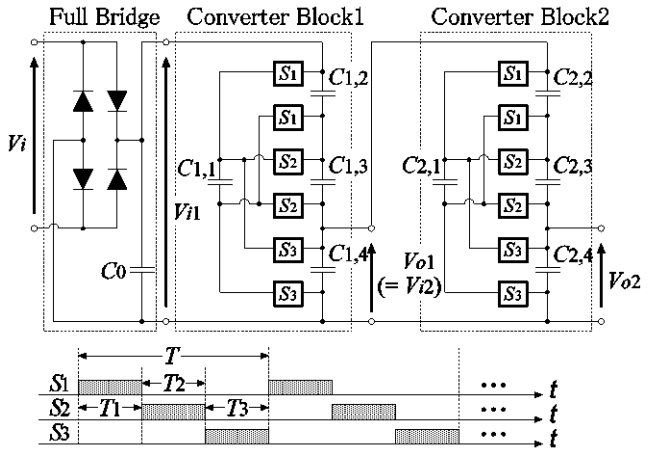

Fig. 1. Circuit configuration of the conventional ac/dc converter

pulses. Since the electric charges stored in the main capacitors are equalized, the voltage of each capacitor becomes 1/3 of the input voltage. By connecting two converter blocks in series, the output voltage V_o becomes 1/9 (= $(1/3)^2$) of the input voltage. However, the capacitor $C_{i,4}$ is charged by $C_{i,1}$ at only one of three states. Therefore, the ripple noise of the conventional converter becomes large. Due to the large ripple noise, the conventional converter of Fig.1 is difficult to achieve high power efficiency.

B. Proposed Converter

Fig. 2 illustrates the circuit configuration of the proposed converter. The proposed converter consists of a full waveform rectifier with a big capacitor and nested voltage equalizers. The operation principle of the proposed converter is as follows: In the voltage equalizer 1, the flying capacitors C_6 and C_7 are connected to the main capacitors C_3 and C_4 in State-T_1. In this timing, the voltages of C_3 becomes same as that of C_4. Next, C_6 and C_7 are connected to the main capacitors C_4 and C_5 in State-T_2. In this timing, the voltages of C_4 becomes same as that of C_5. Therefore, the voltage ratio of capacitors C_3, C_4, and C_5 becomes 1 : 1 : 1. Similarly, in the voltage equalizer 2, the flying capacitors C_8 and C_9 are connected to the main capacitors C_1 and C_2 in State-T_1. In this timing, the voltages of C_1 becomes same as that of C_2. Next, in State-T_2, the flying capacitors C_8 and C_9 are connected to the capacitors C_2 and the series-connected capacitors C_3, C_4, and C_5, respectively. In this timing, the voltages of C_2 becomes same as that of the series-connected capacitors C_3, C_4, and C_5. By repeating these processes, the voltage ratio of capacitors C_1, C_2, C_3, C_4, and C_5 becomes 3 : 3 : 1 : 1 : 1. Therefore, the output V_o becomes

$$V_o = \left(\frac{V_{C5}}{\sum_{k=1}^{5} V_{Ck}}\right)\times V_i = \left\{\frac{V_{C5}}{V_{C5}(3+3+1+1+1)}\right\}\times V_i = \left(\frac{1}{9}\right)V_i \quad (2)$$

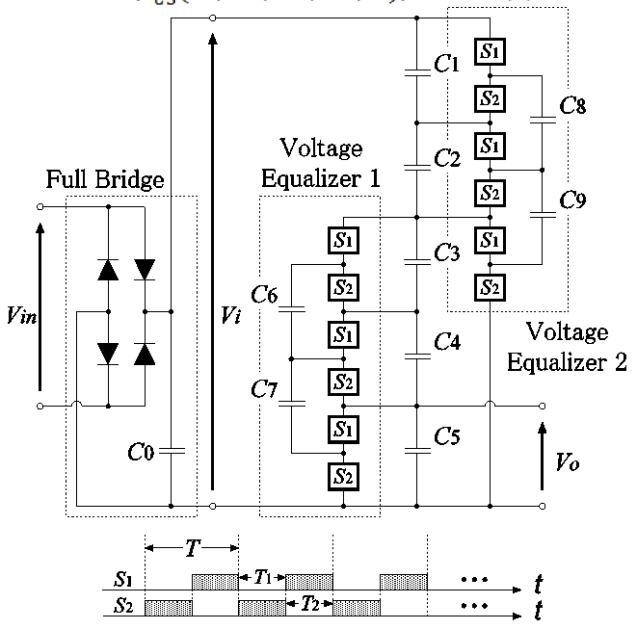

Fig. 2. Circuit configuration of the proposed ac/dc converter

In (2), V_{ck} denotes the voltage of the k-th capacitor. Unlike the conventional SC ac/dc converter [7], the conversion ratio of the proposed converter is expressed as a reverse value of the total sum of V_{ck} ratios. For this reason, the proposed converter can achieve not only simple circuit control but also flexible conversion ratios.

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III. SIMULATION

Concerning the proposed converter realizing the 1/9 step-down conversion, output voltages and power efficiency were demonstrated under conditions that V_{in}=100V@50Hz, T=1μs, R_{on}=0.1Ω, C_0=99μF and $C_{1,k}$=$C_{2,k}$=33μF.

Fig. 3 demonstrates the simulated output voltage of the proposed converter as a function of time. As you can see from Fig. 3, the proposed converter can offer the 1/9 stepped-down DC voltage to the output load R_L (= 100Ω). Of course, the proposed converter can offer various types of output voltages by combing voltage equalizers.

Fig. 4 shows the comparison of output voltages between the proposed converter and the conventional converters [2], [7]. As Fig. 4 shows, the output voltage of the proposed converter is higher than that of the conventional converters. Furthermore, as Table 1 shows, the number of circuit components for the proposed converter is almost the same as that of the conventional converter [7].

Fig. 5 demonstrates the comparison of output ripples between the proposed converter and the conventional converters [2], [7]. As Fig. 5 shows, the proposed converter can achieve smaller ripple noise than the conventional converters. Concretely, the ripple of the proposed converter is less than 7% when the output power is 50W.

Fig. 6 shows the simulated power efficiency as a function of the output power. As you can see from Fig. 6, the power efficiency of the proposed converter is higher than that of the conventional converters. Concretely, the proposed converter can achieve more than 90% efficiency when the output power is less than 50W.

TABLE I: COMPARISON OF THE NUMBER OF CIRCUIT COMPONENTS

	Power switch	Capacitor	Diode	Total
Proposed converter	12	10	4	26
Conventional converter [2]	28	10	4	42
Conventional converter [7]	12	9	4	25

TABLE II: SUMMARY OF COMPARISON RESULTS

	Size	Efficiency	Voltage drop	Ripple
Proposed converter	2	1	1	1
Conventional converter [2]	3	2	2	2
Conventional converter [7]	1	3	3	3

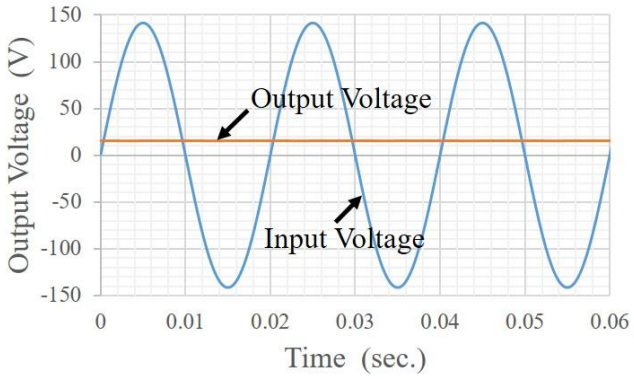

Fig. 3. Simulated output voltage of the proposed converter when the output load is 100Ω.

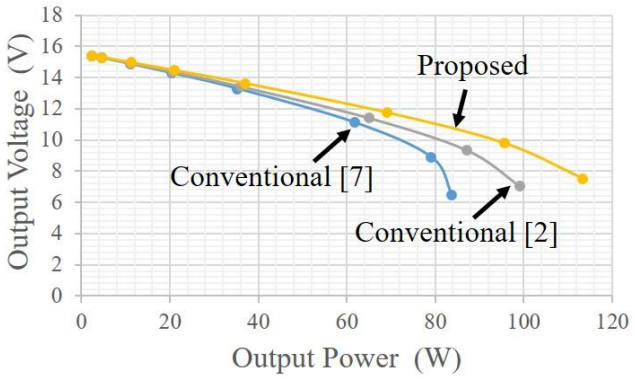

Fig. 4. Simulated output voltages as a function of the output power.

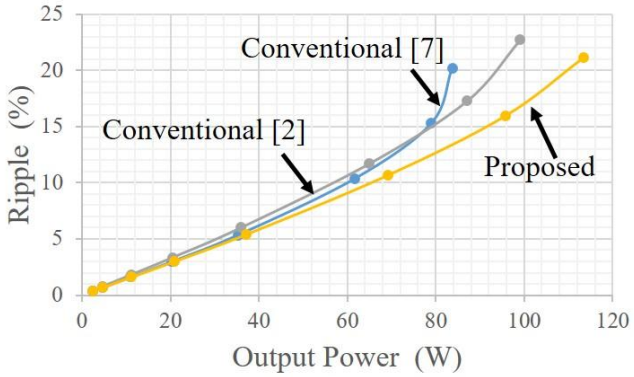

Fig. 5. Simulated ripples as a function of the output power.

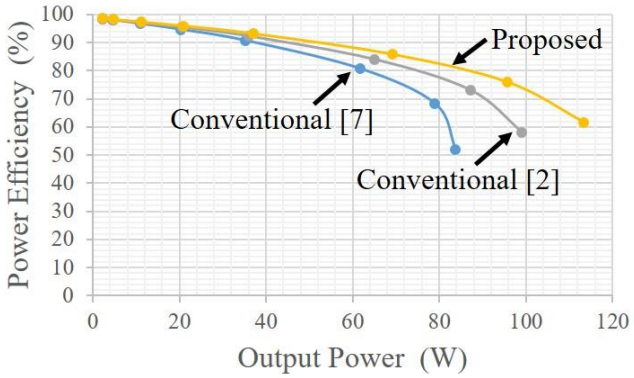

Fig. 6. Simulated power efficiency as a function of the output power

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Table 2 shows the summary of comparison results. Obviously, the proposed converter achieve a better performance than the conventional converters [2], [7] in the point of power efficiency, voltage drop, and ripple noise.

IV. Experiment

To confirm the validity of circuit design, the experimental circuit of the proposed converter was assembled on a breadboard. Table 3 shows the circuit components used in the experimental circuit. In the experimental circuit, a small transformer was connected between the commercial power source and the experimental circuit in order to isolate the power source from the output load. To drive the photo MOS relays, Darlington transistor arrays were connected between the photo MOS relays and the micro-controller that generates clock pulses.

Fig. 7 demonstrates the measured output voltage of the experimental circuit. In Fig. 7, the input voltage was set to V_{in}=141V@60Hz, the period of clock pulses was set to T=100μs, and the turn ratio of the transformer between the primary side and the secondary side was set to 1 : 1. However, due to component fluctuations in the transformer, the practical turn ratio was 1 : 1.13. For this reason, the measured input voltage of Fig. 7 was about 161V (=141V × 1.13). In other words, the input voltage of the experimental circuit is 113V@60Hz. As Fig. 7 shows, the measured output voltage of the proposed converter is about 16.8V when the output load is 10kΩ. Therefore, the feasibility of the proposed converter can be confirmed, because the experimental circuit realized the 1/9 step-down conversion.

TABLE III: Circuit components of the experimental converters

Parts	Components	Models
Full bridge circuit	Diode switch	1N4007
	Capacitor	165μF
Control block	Micro controller	PIC12F1822
	Darlington driver IC	TDG2083APG
	Current control resistance	330Ω
Voltage equalizer	Power switch	AQV212
	Capacitor	33μF
Output load	Resistance	10kΩ

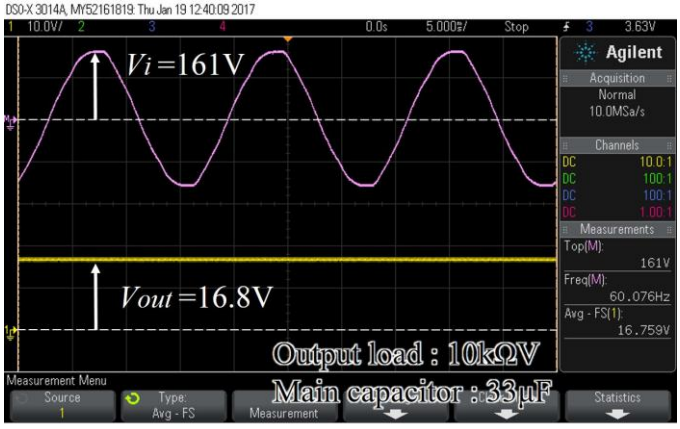

Fig. 7. Measured output voltage of the experimental circuit

V. Conclusion

A novel SC ac/dc converter using nested voltage equalizers has been proposed in this paper. In the proposed converter, a part of the capacitor voltage of the voltage equalizer is converted by other voltage equalizers.

To confirm the validity of circuit design, SPICE simulations were performed concerning the proposed converters realizing 1/9 step-down conversion. The SPICE simulation showed that the proposed converter can achieve more than 90% efficiency and less than 7% output ripple when the output power was less than 50W. Next, in the experiments, we verified the feasibility of the proposed converter by using a breadboard circuit. When the output load was 10kΩ, the experimental circuit generated about 17V DC output by converting a 113V@60Hz AC input. In other words, 1/9 step-down conversion was achieved by the experimental circuit.

The hybrid IC implementation and its experimental analysis are left to a future study. In this work, the proposed converter was not implemented in a hybrid IC form. Therefore, the practical characteristics of the proposed converter including parasitic losses are not clear. In the future study, we are going to conduct the experiments concerning the implemented converter.

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